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Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley, NY 11560

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UNITED STATES PATENT AND TRADEMARK OFFICE

BEFORE THE BOARD OF PATENT APPEALS
AND INTERFERENCES

Ex parte RAJARSHI BHATTACHARYA, SRIRAM GORTI, VINOJ N. KUMAR, CHANDRAMOULEESWARAN SANKARAN, and TIRTHENDU SARKAR

Appeal 2008-002571
Application 10/620,045
Technology Center 2100

Decided[1]: June 15, 2009

Before ALLEN R. MACDONALD, *Vice Chief Administrative Patent Judge*, and HOWARD B. BLANKENSHIP and THU A. DANG, *Administrative Patent Judges*.

BLANKENSHIP, *Administrative Patent Judge*.

DECISION ON APPEAL

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[1] The two-month time period for filing an appeal or commencing a civil action, as recited in 37 C.F.R. § 1.304, begins to run from the decided date shown on this page of the decision. The time period does not run from the Mail Date (paper delivery) or Notification Date (electronic delivery).

STATEMENT OF THE CASE

This is an appeal under 35 U.S.C. § 134(a) from the final rejection of claims 1 and 3-19, which are all the claims remaining in the application. We have jurisdiction under 35 U.S.C. § 6(b).

We affirm.

Invention

Appellants' invention relates to a method, apparatus, and article of manufacture for simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, using a software-based development tool (Fig. 1; Spec. 4:4-14). The method provides, in the software-based development tool, an interface (Fig. 1, 104, Fig. 2, 200; Spec. 4:12, 6:18-24) permitting user control of one or more configurable parameters of the switch fabric (Fig. 2, 216; Spec. 7:22 to 8:2). The method automatically generates, without requiring further user input, a simulation configuration for the switch fabric based on current values of the configurable parameters, the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters (Fig. 5; Spec. 9:12-20).

Representative Claim

1. A method of simulating the operation of at least one switch fabric comprising a plurality of integrated circuits, utilizing a software-based development tool, the method comprising the steps of:

providing in the software-based development tool an interface permitting user control of one or more configurable parameters of the switch fabric; and

automatically generating a simulation configuration for the switch fabric based on current values of the configurable parameters;

the simulation configuration being generated without requiring further user input;

the simulation configuration specifying interconnections between the integrated circuits which satisfy the current values of the configurable parameters.

Prior Art

The Examiner relies on the following references as evidence of unpatentability.

Giancarlo Boggio et al., *NetworkDesigner – Artifex™ - OptSim™: a Suite of Integrated Software Tools for Synthesis and Analysis of High Speed Networks*, Optical Networks Magazine, at 27-41 (Sept/Oct 2001) (hereinafter "Boggio").

Z. Sun, et al., *Simulation Studies of Multiplexing and Demultiplexing Performance in ATM Switch Fabrics*, 10th Teletraffic Symposium, Performance Engineering in Telecommunications Network, at 21/1 to 21/5 (Apr. 14-16, 1993) (hereinafter "Sun").

Kenji Ishida et al., *A 10-GHz 8-b Multiplexer/Demultiplexer Chip Set for the SONET STS-192 System*, IEEE Journal of Solid-State Circuits, Vol. 26, No. 12, at 1936-1943 (Dec 1991) (hereinafter "Ishida").

Examiner's Rejections

Claims 1, 3, 4, and 6-19 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Boggio and Sun.

Claim 5 stands rejected under 35 U.S.C. § 103(a) as being unpatentable over Boggio, Sun, and Ishida.

Claim Groupings

Based on Appellants' arguments in the Appeal Brief, we will decide the appeal on the basis of claims 1, 5, 9, 10, 14, and 15 (*see* 37 C.F.R. § 41.37(c)(1)(vii)).

ISSUES

(1) Have Appellants shown that the combination of Boggio and Sun fails to teach the limitations of claims 1, 9, 10, 14, and 15?

(2) Have Appellants shown that the combination of Boggio, Sun and Ishida fails to teach a designated chip set utilizable in the switch fabric, as recited in claim 5?

FINDINGS OF FACT

Sun

1. Sun uses simulation techniques to study performance of an ATM switch fabric. (Title, Abstract).

2. The switch fabric has a specified number of input links and output links and is built from a number of switching building blocks (Abstract).

3. A basic queuing model is described for switching building blocks. A switch fabric model is built from a number of switching building blocks. Traffic sources are modeled using time series statistical parameters which can be used to model variable bit rate traffic sources. A simulation tool has been developed based on the switch fabric model to carry out simulation studies for a given traffic scenario. (Introduction).

4. The number of inputs and outputs can be defined according to the functions and capacities of the required switching building blocks (Modelling Switching Building Blocks).

5. Switch fabrics can be modeled based on the basic queuing model for the switching building blocks. A mechanism is required to route the cells to their destinations. Each queue is specified by its queue buffer size and queue service rate. (Fig. 2; Modelling Switching Fabrics).

6. Other configurations are also possible, such as introducing more switching queues with more complicated routing mechanisms. More complicated switch fabrics can also be built in the same way using more switching building blocks. Dimensioning the switch fabric is beyond the scope of Sun's study. Sun's paper concentrates on the configuration shown in Fig. 2. (Modelling Switching Fabrics).

7. Based on these simulation models, a simulation tool has been implemented in C language (Simulation Tool).

8. The input of the simulation consists of traffic descriptions of traffic sources, queues, routing, traffic measurement control, and control information. Each traffic source is described by its mean inter-arrival time, the probability distribution function, the queue it attached to and the destination queue it is destined for. Each queue is described by its buffer size and queue service rate. (Simulation Tool).

9. The modeling technique and simulation tool can be used to study different configurations of the switch fabric with different traffic scenarios. It is also useful for studying the dimensions of the buffers needed to balance the cell loss ratio and queuing delay and connection acceptance control with the specified traffic scenario on the switch fabric. (Conclusion).

PRINCIPLES OF LAW

Claim Interpretation

During examination, claims are to be given their broadest reasonable interpretation consistent with the specification, and the language should be read in light of the specification as it would be interpreted by one of ordinary skill in the art. *In re Am. Acad. of Sci. Tech Ctr.*, 367 F.3d 1359, 1364 (Fed. Cir. 2004) (citations omitted). The Office must apply the broadest reasonable meaning to the claim language, taking into account any definitions presented in the specification. *Id.* (citing *In re Bass*, 314 F.3d 575, 577 (Fed. Cir. 2002)).

Obviousness

The question of obviousness is resolved on the basis of underlying factual determinations including (1) the scope and content of the prior art, (2) any differences between the claimed subject matter and the prior art, and (3) the level of skill in the art. *Graham v. John Deere Co.*, 383 U.S. 1, 17 (1966).

The combination of familiar elements according to known methods is likely to be obvious when it does no more than yield predictable results. *KSR Int'l Co. v. Teleflex, Inc.*, 550 U.S. 398, 416 (2007).

ANALYSIS

Section 103 rejection of claims 1, 3, 4, 6-8, 11-13, and 16-19

Appellants argue that Sun assumes a single fixed switch fabric configuration because Sun uses a fixed routing mechanism. Appellants point out that Sun states "'[d]imensioning the switch fabric' beyond the 'simple configuration' involving a single switch fabric is 'beyond the scope' of its disclosure" and infer from this that Sun teaches away from providing an interface permitting user control of one or more configurable parameters of the switch fabric (App. Br. 5; Reply Br. 2). Appellants also contend that Sun and Boggio are not analogous prior art (App. Br. 5; Reply Br. 3-4). Appellants further contend that the motivation for combining Sun and Boggio relies on impermissible hindsight (App. Br. 6; Reply Br. 5-6).

Sun explains, in the passage referenced by Appellants (Sun at 21/3, top), that although only one configuration of a switch fabric was studied in this paper, modifying the switch fabric into other configurations using Sun's

simulation tool was within the ordinary skill of the art (FF 6). In fact, the entire point of Sun's article is to describe a simulation tool that allows a user to test different configurations, dimensions, and parameters of the switch fabric (FF 9).

For example, Sun discloses a switch fabric with a specified number of input links and output links (FF 2). The switch fabric is built from a number of switching building blocks (FF 3). The number of inputs and outputs of the building blocks can be defined according to required functions and capacities (FF 4). Each queue of the switch fabric is specified by its queue buffer size and queue service rate (FF 5). The claim term "user control of one or more configurable parameters" is broad enough to include specifying the number of input and output links, the number of building blocks, the queue buffer size and the service rate as disclosed by Sun.

Furthermore, Sun teaches that a person of ordinary skill in the art was able to configure other parameters of the switch fabric, such as introducing more switching queues with more complicated routing mechanisms and using more building blocks (FF 6, 9). The claim term "user control of one or more configurable parameters" is broad enough to include configuring parameters of the switch fabric, such as introducing more switching queues with more complicated routing mechanisms and using more building blocks as taught by Sun. Therefore, Sun teaches this limitation of claim 1.

The simulation configuration for the switch fabric disclosed by Sun is automatically generated based on current values of the configurable parameters such as the number of input and output links, without requiring further user input, and specifies interconnections between the integrated

circuits which satisfy the current values of the configurable parameters by running the simulation tool implemented in C language (FF 7-9). Therefore, Sun teaches the step of "automatically generating" the simulation configuration as recited in claim 1.

Because Sun, taken alone, teaches all limitations of claim 1, we need not address Appellants' allegation that Sun and Boggio are not analogous prior art, nor do we need to address the allegation that the Examiner failed to articulate a convincing rationale for combining Sun and Boggio.

We therefore sustain the § 103(a) rejection of claims 1, 3, 4, 6-8, 11-13, and 16-19.

Section 103 rejection of claim 9

Appellants contend that Sun does not disclose configurable parameters that comprise a configuration type of the switch fabric (App. Br. 7). The configuration parameters, such as the number of input and output links, form the configuration type of the switch fabric that is modeled and studied by Sun (FF 2, 4-6).

We therefore sustain the § 103(a) rejection of claim 9.

Section 103 rejection of claim 10

Appellants contend that Sun does not teach an interface that permits user selection of one of a centralized configuration, a stackable configuration, and a distributed configuration for the switch fabric (App. Br. 8). The Examiner found that an example of a centralized configuration described by Appellants in the Specification is the same as the exemplary

configuration shown by Sun (Ans. 17-18). Appellants have failed to address this finding by the Examiner. Appellants have also failed to provide any definitions of the centralized, stackable, and distributed configurations that would distinguish this limitation from the configurations taught by Sun.

We therefore sustain the § 103(a) rejection of claim 10.

Section 103 rejection of claim 14

Appellants contend that Sun does not teach a plurality of generators in which each of the generators corresponds to a different configuration of the switch fabric (App. Br. 8-9). However, when Sun generates simulations of different configurations of the switch fabric, the different simulations are generated by the simulation tool using the specific parameters needed to generate the specific configurations (FF 6-9). The plurality of generators corresponding to different configurations of the switch fabric is broad enough to read on generating different simulations of several configurations of a switch fabric as taught by Sun.

We therefore sustain the § 103(a) rejection of claim 14.

Section 103 rejection of claim 15

Appellants contend that Sun does not teach the plurality of generators comprise a centralized configuration generator, a stackable configuration generator, and a distributed configuration generator (App. Br. 9-10). Sun does not include the literal terms "centralized configuration generator, stackable configuration generator, and distributed configuration generator." However, Appellants have given no specific definitions of these words that

prevents this claim limitation from reading on the plurality of configurations that can be generated by the simulation tool of Sun (FF 9). At the least, Appellants have not shown that any of the configurations were unknown to the artisan at the time of invention, and thus would not have been suggested by the teachings of Sun with respect to modeling and simulation of "different configurations" (FF 9).

We therefore sustain the § 103(a) rejection of claim 15.

Section 103 rejection of claim 5

Appellants contend that a designated chip set utilizable in the switch fabric is not taught by the combination of Biggio, Sun, and Ishida.

Sun shows a model for a switch fabric that includes several building blocks (Fig. 2; FF 5). Because the switch fabric is a hardware device, a person of ordinary skill in the art would recognize that the building blocks shown in Sun are models of a chip set utilizable in the switch fabric. The term "designated chip set utilizable in the switch fabric" is broad enough to include the building blocks used in the switch fabric that is modeled by Sun. Appellants have given no explicit definition of the claim term "designated chip set" that excludes this interpretation.

We therefore sustain the § 103(a) rejection of claim 5.

CONCLUSIONS OF LAW

(1) Appellants have not shown that the combination of Boggio and Sun fails to teach the limitations of claims 1, 9, 10, 14, and 15.

(2) Appellants have not shown that the combination of Boggio, Sun, and Ishida fails to teach a designated chip set utilizable in the switch fabric, as recited in claim 5.

DECISION

The Examiner's rejection of claims 1, 3, 4, and 6-19 under 35 U.S.C. § 103(a) as being unpatentable over Boggio and Sun is affirmed.

The Examiner's rejection of claim 5 under 35 U.S.C. § 103(a) as being unpatentable over Boggio, Sun, and Ishida is affirmed.

No time period for taking any subsequent action in connection with this appeal may be extended under 37 C.F.R. § 1.136(a).

AFFIRMED

msc

Ryan, Mason & Lewis, LLP
90 Forest Avenue
Locust Valley NY 11560